Cactus®
Technologies

Industrial Grade PC Card
3XX/3XXP1 Series

Product Manual

Cactus Technologies Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong
Tel: +852-2797-2277
Email: sales@cactus-tech.com

Cactus USA
3112 Windsor Road
Suite A356
Austin, Texas 78703
Tel: +512-775-0746
Email: americas@cactus-tech.com

Cactus-Tech.com

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01 Introduction to Cactus Technologies Industrial Grade PC Card -3XX/-3XX-P1/-3XX-WP1 Series Products

Features

- Solid state design with no moving parts
- Industry standard PC Card Type II form factor
- Supports TrueIDE Mode
- Supports ATA PIO Modes 0-4 in TrueIDE Mode
- Supports MultiWord DMA Modes 0-2 in TrueIDE Mode
- Supports UDMA Modes 0-4 in TrueIDE Mode
- High reliability, MTBF > 4,000,000 hrs.
- Enhanced error correction, < 1 error in 10^{14} bits read
- Intelligent power management to reduce power consumption
- Dual voltage support: 3.3V/5.0V

Overview

The Cactus Technologies PC Card is a high capacity solid-state flash memory product that complies with the Personal Computer Memory Card International Association (PCMCIA) ATA (PC Card ATA) standard. It also supports True IDE Mode, which is electrically compatible with an IDE disk drive. PC Cards provide up to 32GB of formatted storage capacity in the PC Card Type II form factor.

The Cactus Technologies Industrial Grade PC Card products use high quality flash memory from well known vendors, such as Samsung Corporation. In addition, it include an on-card intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller's firmware is upgradeable, thus allowing feature enhancements and firmware updates in the field.

Additional features for 3XXP1 series

- ATA Security Feature Set
- CTLock™. This feature allows the card to be locked to a specific host.
- CTPurge™. This feature allows the host to securely erase the contents of the card using procedures in published standards.
- CTWProt™. This feature allows for software initiated write protect function.

1.1. Supported Standards

Cactus Technologies CompactFlash Memory Cards are fully electrically compatible with the following specifications:

- PCMCIA PC Card Standard v7.0
- PCMCIA PC Card ATA Specification v7.0
- ATA Specification published by ANSI: X3.221 AT Attachment Interface for Disk Drives

1.2. Product Features

Cactus Technologies Industrial Compact Flash Cards contain a high level, intelligent controller. This intelligent controller provides many capabilities not found in other types of memory cards. These capabilities include the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies Industrial PC Cards appears as a standard ATA disk drive to the host system. The card utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the card as per the ATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the card. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies Industrial PC Card products today will continue to work with future Cactus Technologies Industrial PC cards built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies Industrial PC cards contain a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies Industrial PC cards is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the card has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies Industrial PC cards unparalleled reliability.

1.2.3. Intelligent Power Management

Cactus Technologies Industrial PC cards employ sophisticated power management algorithms to conserve power. Upon completion of a command, the card will automatically enter sleep mode if no further commands are received. In most situations, the card will be in sleep mode except when the host is accessing it, thus conserving power. When the card is in sleep mode, any command issued to the card will cause it to exit sleep and respond.

1.2.4. Power Supply Requirements

This is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ±10% or 5.00 volts ± 10%. Per the PCMCIA specification Section 2.1.1, the host system must apply 0 volts in order to change a voltage range. This same procedure of providing 0 volts to the card is required if the host system applies an input voltage outside the desired voltage by more than 20%. This means less than 4.0 volts for the 5.00 volt range and less than 2.70 volts for the 3.30 volt range.

02 Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus PC Card Products
Temperature	**Operating:**	0° C to +70° C (Standard) -45° C to +90° C (Extended)
Humidity	**Operating & Non-Operating:**	8% to 95%, non-condensing
Acoustic Noise		0 dB
Vibration	**Operating & Non-Operating:**	20 G peak to peak maximum
Shock	**Operating & Non-Operating:**	3,000 G maximum
Altitude (relative to sea level)	**Operating & Non-Operating:**	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Industrial PC Card Products
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		3.3V or 5.0V ±10%
(Maximum Average Value) See Notes.		
2GB or lower capacities	**Sleep:** **Reading:** **Writing:**	250 µA 85 mA 85 mA
4GB or higher capacities	**Sleep:** **Reading:** **Writing:**	500uA 220mA 180mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all card inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the card controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Start Up Times	**Reset to ready:**	35 msec typical
Read Transfer Rate	**Operating &Non-Operating:**	up to 35.0 Mbytes/sec*
Write Transfer Rate		up to 20.0 Mbytes/sec *
Controller Overhead	**Command to DRQ**	2 msec maximum

* Please note that for maximum performance in TrueIDE UDMA modes, proper termination and PCB layout guidelines as described in the ATA specifications must be followed to minimize signal integrity problems. Maximum transfer rates are achieved on 2GB or higher capacity cards.

2.4. System Reliability

Table 2-4. Reliability

MTBF (@ 25°C)	>4,000,000 hours
Data Reliability	<1 non-recoverable error in 10^{14} bits READ
Endurance:	>2,000,000 erase/program cycles

2.5. Physical Specifications

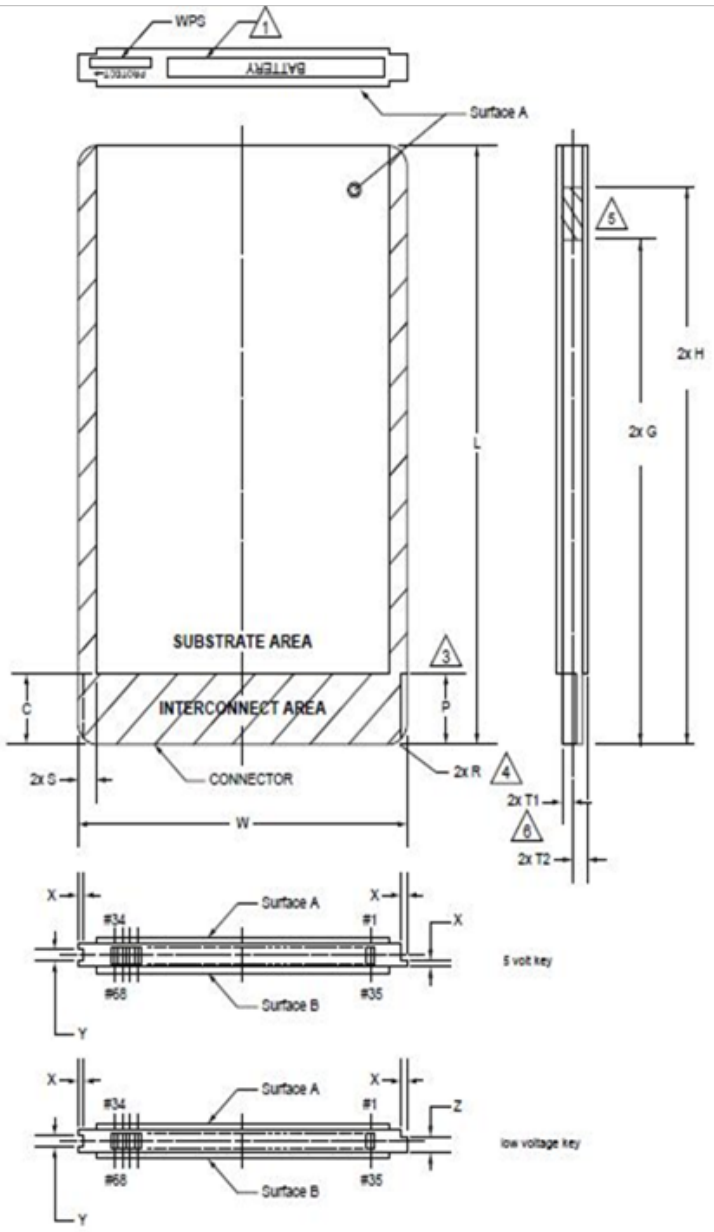
The following sections provide the physical specifications for Cactus Technologies Industrial PC Card products.

2.5.1. PC Card Physical Specifications

Refer to Table 2-5 and see Figure 2-1 for PC Card physical specifications and dimensions.

Table 2-5. PC Card Physical Specifications	**PC Card**
Weight:	43 g. (1.52 oz.) maximum
Length:	85.6 ± 0.20 mm (3.370 ± .008 in.)
Width:	54.0 ± 0.10 mm (2.126 ± .004 in.)
Thickness:	5.0 mm max. (.1968 in.)

Figure 2-1. PC Card Type II Dimensions



C MIN	L ± 0.20	P MIN 3	R ± 0.10 4	S MIN	T1 ± 0.05 5	T2 MAX	W ± 0.10	X ± 0.05	Y ± 0.05	Z ± 0.05	G ± 0.60	H ± 0.60
10.0	85.60	10.0	0.60	3.0	1.65	2.50	54.00	1.00	1.60	2.10	65.60	79.60

1. RECOMMENDED BATTERY LOCATION. THE BATTERY HOLDER SHOULD BE DESIGNED SO THAT THE POSITIVE SIDE OF THE BATTERY IS UP (TOWARD SURFACE A)
2. THE PC CARD SHALL BE OPAQUE (NON SEE THRU)
3. POLARIZATION KEY LENGTH
4. DIMENSION R CORNER RADIUS
5. GROUND CLIP LOCATION

03 Capacity Specifications

The following sections provide capacity specifications for Cactus Technologies PC Card products.

3.1. PC Card Capacity Specifications

Table 3-6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 3-6. Model Capacities

Capacity	Capacity (formatted)	Sectors/ Card (Max LBA+1)	No. of Heads	No. of Sectors/Track	No. of Cylinders
128MB	**129,761,280 bytes**	253,440	8	32	990
256MB	**259,522,560 bytes**	506,880	16	32	990
512MB	**521,256,960 bytes**	1,018,080	16	63	1,010
1GB	**1,047,674,880 bytes**	2,046,240	16	63	2,030
2GB	**2,097,930,240 bytes**	4,097,520	16	63	4,065
4GB	**4,224,245,760 bytes**	8,250,480	16	63	8,185
8GB	**8,456,749,056 bytes**	16,517,088	16	63	16,386
16GB	**16,829,890,560 bytes**	32,870,880	16	63	32,610
32GB	**32,978,534,400 bytes**	64,411,200	16	63	63,900

04 Interface Description

The following sections provide detailed information on the Cactus Technologies Industrial PC Card interface.

4.1. PC Card Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4-7. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

Table 4-7. PC Card Pin Assignments and Pin Type

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A102	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10			10			10		
11	A09	I	11	A09	I	11	A092	I
12	A08	I	12	A08	I	12	A082	I
13			13			13		
14			14			14		I
15	-WE	I	15	-WE	I	15		
16	RDY/BSY	O	16	IREQ	O	16	INTRQ	O
17	VCC		17	VCC		17	VCC	I
18	VPP		18	VPP		18		
19			19			19		
20			20			20		
21			21			21		
22	A07	I	22	A07	I	22	A072	I
23	A06	I	23	A06	I	23	A062	I
24	A05	I	24	A05	I	24	A052	I
25	A04	I	25	A04	I	25	A042	I
26	A03	I	26	A03	I	26	A032	I
27	A02	I	27	A02	I	27	A02	I
28	A01	I	28	A01	I	28	A01	I
29	A00	I	29	A00	I	29	A00	I
30	D00	I/O	30	D00	I/O	30	D00	I/O

PC Card Memory Mode		
Pin Num	Signal Name	Pin Type
31	D01	I/O
32	D02	I/O
33	WP	O
34	GND	
35	GND	
36	-CD1	O
37	D111	I/O
38	D121	I/O
39	D131	I/O
40	D141	I/O
41	D151	I/O
42	-CE21	I
43	-VS1	O
44	-IORD	I
45	-IOWR	I
46		
47		
48		
49		
50		
51	VCC	
52	VPP	
53		
54		
55		
56	-CSEL	I
57	-VS2	O
58	RESET	I
59	-WAIT	O
60	-INPACK	O
61	-REG	I
62	BVD2	I/O
63	BVD1	I/O
64	D081	I/O
65	D091	I/O
66	D101	I/O
67	-CD2	O
68	GND	

PC Card I/O Mode		
Pin Num	Signal Name	Pin Type
31	D01	I/O
32	D02	I/O
33	-IOIS16	O
34	GND	
35	GND	
36	-CD1	O
37	D111	I/O
38	D121	I/O
39	D131	I/O
40	D141	I/O
41	D151	I/O
42	-CE21	I
43	-VS1	O
44	-IORD	I
45	-IOWR	I
46		
47		
48		
49		
50		
51	VCC	
52	VPP	
53		
54		
55		
56	-CSEL	I
57	-VS2	O
58	RESET	I
59	-WAIT	O
60	-INPACK	O
61	-REG	I
62	-SPKR	I/O
63	-STSCHG	I/O
64	D081	I/O
65	D091	I/O
66	D101	I/O
67	-CD2	O
68	GND	

True IDE Mode		
Pin Num	Signal Name	Pin Type
31	D01	I/O
32	D02	I/O
33	-IOCS16	O
34	GND	
35	GND	
36	-CD1	O
37	D11	I/O
38	D12	I/O
39	D13	I/O
40	D14	I/O
41	D15	I/O
42	-CS1	I
43	-VS1	O
44	-IORD HSTROBE5 -HDMARDY6	I
45	-IOWR STOP7	I
46		
47		
48		
49		
50		
51	VCC	
52	VPP	
53		
54		
55		
56	-CSEL	I
57	-VS2	O
58	-RESET	I
59	IORDY -DDMARDY5 DSTROBE6	O
60	-DMARQ	O
61	-DMACK	I
62	-DASP	I/O
63	-PDIAG	I/O
64	D081	I/O
65	D091	I/O
66	D101	I/O
67	-CD2	O
68	GND	

NOTES:
1. These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. Please refer to Section 3.3 for definitions of input/output types
5. Signal usage when UDMA write mode is active
6. Signal usage when UDMA read mode is active
7. Signal usage when UDMA mode is active

4.2. Signal Description

The Cactus Technologies Industrial PC Card products can be configured to operate in either I/O mode or memory mode as per the PCMCIA Release 2.1 specification. The configuration of the PC Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the PC Card. The Cactus Technologies Industrial PC Card also supports a TrueIDE mode. This mode is entered by grounding the –OE pin on power up.
Table 4-8 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the PC Card sources are outputs. The PC Card logic levels conform to those specified in the PCMCIA Release 2.1 Specification.

Table 4-8. Signal Description

Signal Name	Dir.	Description
A10—A0 (PC Card Memory Mode) A10—A0 (PC Card I/O Mode)	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the PC Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal.
A2—A0 (True IDE Mode) A10—A3 (True IDE Mode)		In True IDE Mode only A[2:0] is used to select the one of eight registers in the Task File. In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed		This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)		In True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.

Signal Name	Dir.	Description
-SPKR (PC Card I/O Mode)	I/O	This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)		In True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	These Card Detect pins are connected to ground on the PC Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)		This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)		This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2 always accesses the odd byte of the word. CE1 accesses the even byte or the Odd byte of the word depending on A0 and CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 3-11, 3-12, 3 15, and 3-16.
-CE1, -CE2 (PC Card I/O Mode) Card Enable		This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)		In True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)		This signal is not used for this mode.
-CSEL (True IDE Mode)		This internally pulled up signal is used to configure this device as a Master or a Slave when configured in True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal Name	Dir.	Description
D15—D00 (PC Card Memory Mode)	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15—D00 (PC Card I/O Mode)		These signals are the same as the PC Card Memory Mode signal.
D15—D00 (True IDE Mode)		In True IDE Mode all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND (PC Card Memory Mode)	--	Ground.
GND (PC Card I/O Mode)		This signal is the same for all modes.
GND (True IDE Mode)		This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge		The Input Acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
-DMARQ (TureIDE Mode) DMA request		In TrueIDE Mode, this ss DMA request from the device for either MWDMA or UDMA operations.
-IORD (PC Card Memory Mode)	I	This signal is not used in this mode.
-IORD (PC Card I/O Mode)		This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode, UDMA not active) -HDMARDY (TrueIDE Mode, UDMA write) HSTROBE (TrueIDE mode, UDMA read)		In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in PC Card I/O Mode. In TrueIDE Mode, when UDMA write is active, this signal is asserted by the host to indicate that it is ready to receive data in bursts. In TrueIDE Mode, when UDMA read is active, this signal is the data out strobe sent by the host; data is latched by the device on both rising and falling edges of this signal.

Signal Name	Dir.	Description
-IOWR (PC Card Memory Mode)	I	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)		The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode, UDMA not active) STOP (TrueIDE Mode, UDMA active)		In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in PC Card I/O Mode. In TrueIDE Mode, when UDMA protocol is active, host asserts this signal to terminate UDMA transfers.
-OE (PC Card Memory Mode)	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the PC Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)		In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)		To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	In Memory Mode this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)		I/O Operation—After the PC Card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)		In True IDE Mode, this signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.

Signal Name	Dir.	Description
-REG (PC Card I/O Mode)	I	The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (TrueIDE Mode)		In TrueIDE mode, this is an input from the host to signal to the device that its DMA request has been acknowledged.
RESET (PC Card Memory Mode)	I	When the pin is high, this signal resets the PC Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)		This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)		In True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)		This signal is the same for all modes.
VCC (True IDE Mode)		This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	Voltage Sense Signals. -VS1 is grounded so that the PC Card CIS can be read at 3.3 volts and VS2 is open and reserved by PC Card for a secondary voltage.
-VS1 -VS2 (PC Card I/O Mode)		This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)		This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	The –WAIT signal is driven by the PC Card to signal to the host to delay completion of the memory cycle in progress.

Signal Name	Dir.	Description
-WAIT (PC Card I/O Mode)	O	The –WAIT signal is driven by the PC Card to signal to the host to delay completion of the I/O cycle in progress.
-IORDY (True IDE Mode, UDMA not active) -DDMARDY (TrueIDE Mode, UDMA write active) DSTROBE (TrueIDE Mode, UDMA read active)		In TrueIDE Mode, when UDMA protocol is not active, the -IORDY signal is driven by the PC Card to extend the I/O cycle in progress. In TrueIDE Mode, when UDMA write protocol is active, this signal is driven by the device to indicate that it is ready to receive data out bursts. In TrueIDE Mode, when UDMA read protocol is active, this signal is the data strobe sent by the device to the host; data is latched by the host on both rising and falling edges of this signal.
-WE (PC Card Memory Mode)	I	This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)		In PC Card I/O Mode, this signal is used for writing the configuration registers.
Reserved (True IDE Mode)		In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect	O	Memory Mode—The PC Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)		I/O Operation—When the PC Card is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)		In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4.3. Electircal Specification

The following table defines all D.C. Charactaristics for the PC Card Series. Unless otherwise stated, conditions are:

Vcc = 5V ± 10% or Vcc = 3.3V ± 10%
Ta = -45°C to 90°C

4.3.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-65	+150	oC
Operating Temperature	TA	-45	+90	oC
Vcc with respect to GND	Vcc	-0.3	6.5	V

4.3.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	ILI	-10	10	uA
Output Leakage Current	ILO	-10	10	uA
Input/Output Capacitance	CI/Co		10	pF
Operating Current Sleep Mode: 2GB or below 4GB or above Active: 2GB or below 4GB or above	Icc		 0.3 0.6 120 280	 mA

4.3.3. AC Characteristics

Please refer to the PCMCIA PC Card Standard v7.0 for complete AC timing specifications for the various modes.

4.4. Card Configuration

The PC Card is identified by information in the Card Information Structure (CIS). The entries in Table 4-9 and Table 4-10 show how to access the various registers and address spaces in the memory cards.

Table 4-9. Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table 4-10. Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)

NOTES:
The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the PC Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.4.1. Attribute Memory Function

Attribute memory is a space where PC Card CIS and configurations registers are stored, and is limited to 8-bit wide accesses only at even addresses.

As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 4-11 for signal states and bus validity for the Attribute Memory function.

Table 4-11. Configuration Registers Decoding

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM									
(8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Do not care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Do not care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Do not care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Do not care	Even Byte

NOTES:
The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.4.2. Configuration Option Register (Address 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the PC Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset—Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the PC Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the PC Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PC Card Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5—Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the PC Card as shown below.

NOTE: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 4-12. Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

4.4.3. Card Configuration and Status Register (Address 202h in Attribute Memory)

The Card Configuration and Status Register contain information about the Card's condition.

Table 4-13. Card Configuration and Status Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the PC Card is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the PC Card is configured for I/O.

IOis8 The host sets this bit to a one (1) if the PC Card is to be configured in an 8-bit I/O mode. The PC Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the PC Card to be in the power saving or active mode. When the bit is one (1), the PC Card enters a power down mode. When zero (0), the host is requesting the PC Card to enter the active mode. The PC Card Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The PC Card automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4.4. Pin Replacement Register (Address 204h in Attribute Memory)

Table 4-14. Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RRdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

RWProt This bit is always zero (0) since the PC Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 4-15. Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.4.5. Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Table 4-16. Socket and Copy Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the PC Card.

4.5. I/O Transfer Function

The I/O transfer to or from the PC Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal IOIS16 is asserted by the PC Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16-bit transfer is attempted, and the IOIS16 signal is not asserted by the PC Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The PC Card permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the PC Card responds (refer to Table 4-17).

Table 4-17. I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L	H	L	L	L	H	High Z	Even-Byte
	L	H	L	H	L	H	High Z	Odd-Byte
Byte Output Access (8 bits)	L	H	L	L	H	L	Do not care	Even-Byte
	L	H	L	H	H	L	Do not care	Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Do not care	Do not care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Do not care

4.6. Common Memory Transfer Function

The Common Memory transfer to or from the PC Card can be either 8 or 16 bits. The PC Card permit both 8- and 16-bit accesses to all of its Common addresses (refer to Table 4-18).

Table 4-18. Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H	H	L	L	L	H	High Z	Even-Byte
	H	H	L	H	L	H	High Z	Odd-Byte
Byte Write Access (8 bits)	H	H	L	L	H	L	Do not care	Even-Byte
	H	H	L	H	H	L	Do not care	Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Do not care

4.7. True IDE Mode I/O Transfer Function

The PC Card can be configured in a True IDE Mode of operation. This PC Card is configured in this mode only when the -OE input signal is grounded by the host when power is applied to the card. In True IDE Mode, the PC Card protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In addition, No Memory or Attribute Registers are accessible to the host.

NOTE: Removing and reinserting the PC Card while the host computer's power is on will reconfigure the PC Card to PC Card ATA mode from the original True IDE Mode. To configure the PC Card in True IDE Mode, the 50-pin socket must be power cycled with the PC Card inserted and -OE (output enable) grounded by the host.

Table 4-19 defines the function of the operations for the True IDE Mode.

Table 4-19. IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

05 ATA Drive Register Set Definition and Protocol

The PC Card can be configured as a high performance I/O device through the following ways:

- Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16-byte I/O block using any available IRQ.
- Memory space.

The communication to or from the PC Card is done using the Task File registers, which provide all the necessary registers for control and status information. The PC Card interface connects peripherals to the host using four register mapping methods. Table 5-20 is a detailed description of these methods.

Table 5-20. I/O Configurations

Standard Configurations				
Config Index	**IO or Memory**	**Address**	**Drive #**	**Description**
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

5.1. I/O Primary and Secondary Address Configurations

Table 5-21. Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte access to register 0 with CE1 high and CE2 low accesses the error (read) or feature (write) register.

5.2. Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the PC Card, the registers are accessed in the block of I/O space decoded by the system in Table 5-22.

Table 5-22. Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

NOTES:
1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to register 0 with CE1 high and CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines that are not indicated are ignored by the PC Card for accessing all the registers in this table.

5.3. Memory Mapped Addressing

When the PC Card registers are accessed via memory references, the registers appear in the common memory space window: 0 2K bytes as shown in Table 5-23.

Table 5-23. Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

NOTES:
1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the PC Card.

5.4. True IDE Mode Addressing

When the PC Card is configured in the True IDE Mode the I/O decoding is as listed in Table 5-24.

Table 5-24. True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

5.5. ATA Registers

NOTE: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

5.5.1. Data Register (Address-1F0[170]; Offset 0, 8, 9)

The Data Register is a 16-bit register, and it is used to transfer data blocks between the PC Card data buffer and the Host. This register overlaps the Error Register. Table 5-25 describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 7.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

NOTE: Because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. Accesses to these locations are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Table 5-25. Data Register

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error/Feature Register	1	0	1	1, Dh	D7-D0
Error/Feature Register	0	1	X	1	D15-D8
Error/Feature Register	0	0	X	Dh	D15-D8

5.5.2. Error Register (Address-1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

5.5.3. Feature Register (Address-1F1[171]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the PC Card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with CE2 low and -CE1 high (except in True IDE Mode operation).

5.5.4. Sector Count Register (Address-1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the PC Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

5.5.5. Sector Number (LBA 7-0) Register (Address-1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any PC Card data access for the subsequent command.

5.5.6. Cylinder Low (LBA 15-8) Register (Address-1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

5.5.7. Cylinder High (LBA 23-26) Register (Address-1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

5.5.8. Drive/Head (LBA 27-24) Register (Address 1F6[176]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected When DRV=1, drive (card) 1 is selected. In PCMCIA Mode operation, Card 0 or 1 is selected using the copy field of the PC Card Socket and Copy configuration register.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

5.5.9. Status and Alternate Status Registers (Address 1F7[177] and 3F6[376]; Offsets 7 and Eh)

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the Industrial ATA product has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the Industrial ATA product is ready to accept a command.
Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC) This bit is set when the Industrial ATA product is ready.
Bit 3 (DRQ) The Data Request is set when the Industrial ATA product requires that information be transferred either to or from the host through the Data register.
Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX) This bit is always set to 0.
Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

5.5.10. Device Control Register (Address-3F6[376]; Offset Eh)

This register is used to control the card interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (Do not care).
Bit 6 This bit is an X (Do not care).
Bit 5 This bit is an X (Do not care).
Bit 4 This bit is an X (Do not care).
Bit 3 This bit is ignored by the card.
Bit 2 (SW Rst) This bit is set to 1 in order to force the card to perform an AT Disk controller Soft Reset operation. This does not change the PC Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The card remains in Reset until this bit is reset to '0'.
Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.
Bit 0 This bit is ignored by the card.

5.5.11. Card (Drive) Address Register (Address 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the Industrial ATA product. Following are some possible solutions to this problem for the PC Card implementation:
1. Locate the Industrial ATA product at a non-conflicting address (i.e., Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and an Industrial ATA product in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when an Industrial ATA product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the Industrial ATA product's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the Industrial ATA product or b) if provided use an additional Primary/Secondary configuration in the Industrial ATA product that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

06 -3XXP Firmware Specifications

The following sections describe in detail the enhanced firmware features available only in the Cactus Technologies -3XXP PC Card devices.

6.1. ATA Mode Security Feature Set

This feature set implements all the required commands of the ATA Security Mode Feature Set as defined in the ATA7 specifications. These commands are:

- · Security Set Password (F1h)
- · Security Unlock (F2h)
- · Security Erase Prepare (F3h)
- · Security Erase Unit (F4h)
- · Security Freeze Lock (F5h)
- · Security Disable Password (F6h)

Note that these are not Vendor Specific commands but rather an optional ATA feature set as documented in the ATA specifications. Please refer to the official ATA 7 documentation, INCITS 397-2005 (1532D), for details and specifics. The Cactus 303Pro implementation follows completely the command descriptions and state transitions as described in the ATA7 documentation.

6.2. CTLock™

The CTLock™ feature allows a Cactus Technologies flash card/drive to be locked to a specific host. This can be used as a basic access control or IP protection mechanism and is a simple way to implement a drive lock function without the host having to implement the full ATA Security Feature Set. Note that it is recommended that the user implements either CTLock™ or the ATA Security Feature Set but not both at the same time.

The way the CTLock™ feature works is that the host, after having read the drive's Identify Drive information, which contains the drive's unique serial number and other Cactus specific data, can then generate an unique Lock code, which it can then write into the drive. Once this Lock code is written using the CTLock™ command, the drive will default to 'VS Locked' mode upon the next power up or hard reset. The drive will not respond to any non-diagnostic ATA command until the host sends over the unlock code using the CTLock™ command. If the drive is unplugged from the original host system and plugged into a different host, data on the drive will not be accessible by the new host unless the new host also issues the CTLock™ command with the proper Lock code and the Unlock bit set.

The host can disable the CTLock™ feature by setting the Lock Erase bit using the CTLock™ command with the proper Lock code.

6.2.1. Command Structure

CTLock™ command is a Vendor Specific ATA Command with the following task file structure:

Register	7	6	5	4	3	2	1	0
Feature	Reserved					Lock Erase	Unlock	Lock
Sector Count	01h							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Drive/Head	1	0	1	D	0	0	0	0
Command	83h							

CTLock™ is a PIO Data Out command. Upon issuing the command and receiving a data ready status from the drive, the host will send over 1 sector (512bytes) of data. The format of this data is as follows:

byte	Description
00-31	zeroes
32-64	Lock code
65-511	zeroes

If this command is issued with Bit 0 of Feature Reg. set, the drive will enable the VS Lock mode. In this mode, the drive will not response to normal ATA data transfer commands until a CTLock™ command is issued with the same Lock code and the Unlock bit set. The only ATA commands that the drive will execute when in VS Lock mode are the following:

Command	Opcode
Check Power Mode	E5h
Execute Drive Diagnostic	90h
Identify Drive	ECh
Idle	E3h
Idle Immediate	E1h
NOP	00h
Read Buffer	E4h
Set Features	EFh
Set Multiple Mode	C6h
Sleep	E6h
Standby	E2h
Standby Immediate	E0h
Write Buffer	E8h

If the CTLock™ command is issued with the Lock code and bit 2 of Feature Reg. set, the previously saved Lock code will be erased and the drive will revert back to normal operation with VS Lock disabled. To re-enable the VS Lock mode, the host must reissue a CTLock™ command with a Lock code and the Lock bit set.

Note that bits 0,1 & 2 of the Feature Reg. are mutually exclusive. If the CTLock™ command is issued with more than one of the above 3 bits set, the command will be rejected and an error status returned.

The current status of CTLockä is reported in Identify Drive word 128 bits 10 & 11 as follows:

Bit 11 (lock)	Bit 10 (enable)	Description
0	0	CTLock is disabled
0	1	CTLock is enabled, drive is unlocked
1	1	CTLock is enabled, drive is locked

6.3. CTPurge™

This feature allows the host to issue a single command and erase all the content of the flash card/drive. There are various options available to control how thoroughly the erasure is to be carried out, so that it can meet various published standards. This operation will erase all data on the flash, including bad blocks, internal data structures, re-assigned blocks and reserve blocks. After the CTPurge™ operation, the card/drive will no longer be accessible by the host and must be replaced.

The drive's firmware keeps track of the status of the CTPurge™ operation. If power is interrupted while CTPurge™ is in progress, the purge operation will resume when power is reapplied.

6.3.1. Command Structure

The host can initiate a CTPurge™ operation by issuing the following Vendor Specific Command:

Register	7	6	5	4	3	2	1	0
Features	Count							
Sector Count	Opcode							
Sector Number	Parameter 1							
Cylinder Low	Parameter 2							
Cylinder High	Reserved							
Drive/Head	1	0	1	D	0	0	0	0
Command	82h							

The Opcode field is partitioned into groups of 2 bits each with the following definitions:

bit[7:6] These two bits determine how many sequences to perform. The coding is as follows:

00 1 sequence
01 2 sequences
10 3 sequences
11 reserved

bit[5:4] These two bits determine the type of operation to be performed for sequence 3. The coding is as follows:

- 00 erase only
- 01 erase and overwrite with random data
- 10 erase and overwrite with character defined in parameter 1
- 11 erase and overwrite with character defined in parameter 2

bit[3:2] These two bits determine the type of operation to be performed for sequence 2. The coding is the same as for sequence 3.

bit[1:0] These two bits determine the type of operation to be performed for sequence 1. The coding is the same as for sequence 3.

For sequence 1, an optional 'count' can be specified. If count=0, the sequence is performed only once. For non-zero counts, the sequence is repeated for count+1 times.

By default, if none of the optional parameters are specified, the firmware will perform an erase only operation when this command is issued.

6.3.2. Standard Compliance

The CTPurge™ command structure allows the operation to meet a variety of specified sanitizing procedures. The table below shows the command entry for each type of specified sanitizing procedure.

Operation	Opcode	Parameter 1	Parameter 2	Count
Erase only (default)	0x00	0x00	0x00	0x00
Erase and overwrite with random data once	0x01	0x00	0x00	0x00
Erase and overwrite with random data N times	0x01	0x00	0x00	N-1
USA-AF AFSSI 5020 Erase and overwrite with zeroes, then erase and overwrite with ones, then erase and overwrite with random data	0x9E	0x00	0xFF	0x00
USA Navy NAVSO P-5239-26 Erase and overwrite with random data, then erase and overwrite with random data again	0x45	0x00	0x00	0x00
DoD 5220.22-M Erase and overwrite with single character, then erase again	0x42	Character	0x00	0x00
NSA Manual 130-2 Erase and overwrite with random character 2 times, then erase and overwrite with a character	0x49	Character	0x00	0x00

Operation	Opcode	Parameter 1	Parameter 2	Count
NSA Manual 9-12 Erase and overwrite with single character	0x02	Character	0x00	0x00
USA-Army 380-19 Erase and overwrite with random data, erase and overwrite with a character, then erase and overwrite with complement of the character	0xb9	Character	Complement of Character	0x00
NISPOMSUP Chap.8, Sect.8-501 Erase and overwrite with a character, its complement, and then random data	0x9e	Character	Complement of Character	0x00
IREC (IRIG) 106 Erase and overwrite with 0x55, then erase and overwrite with 0xAA, then erase	0x8e	0x55	0xAA	0x00

6.3.3. Status Reporting

When CTPurge™ is completed, the drive will return ready status but will no longer be able to process any new ATA commands as all internal firmware has been erased.

6.3.4. Time and Power Requirements

The time required to perform a CTPurge™ operation depends on the capacity of the drive and the type of purge operation that is being performed. The host should ensure that power to the card/drive is maintained for the entire duration during the purge process. The following table lists some typical numbers that can be expected.

Capacity	Default Purge	DoD 5220.22-M	NSA 130-2
4GB	12s	3min. 28s	13min. 15s
8GB	23s	7min. 8s	26min. 51s
16GB	47s	15min. 45s	59min. 55s
32GB	43s	24min. 31s	95min 30s

The power consumption during a CTPurge™ operation is also dependent on drive capacity, the type of purge operation requested and, to a lesser extent, the particular overwrite pattern used. Some typical numbers are shown below:

Capacity	Power Consumption (default Purge)
4GB	79mA
8GB	82mA
16GB	79mA
32GB	81mA

6.4. CTWPROT™

CTWPROT™ enables write protect function on the entire Cactus Technologies card/drive. This feature is activated in software.

The write protect function can be toggled on/off by the user during use in the field. When the write protect function is activated, all subsequent Write commands that attempt to store data to the flash memory will be aborted and an Error status will be returned to the host. As there is no predefined way of handling write aborts in the ATA standard, the host will need to have a special driver/handler to properly handle such situations. The Cactus Technologies card/drive supports the ATA Request Sense command (03H). This command is now obsolete but was used in earlier ATA standards for the drive to report extended error codes. If the host issues this command immediately following a write abort, the command will complete and the Cactus Technologies drive will return an extended error code of 27H in the Error register to indicate to the host that there is a write protect violation. This then allows the host application to display an appropriate error message to the user instead of just hanging the system on a write abort situation.

6.4.1. Command Structure

The CTWPROT™ command is a Vendor Specific Command with the following task file structure:

Register	7	6	5	4	3	2	1	0
Feature	Reserved							
Sector Count	command code							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Drive/Head	1	1	1	D	0	0	0	0
Command	C2h							

CTWPROT™ is a non data transfer command. The usage of the command code is as follows:

12d: enable write protect

13d: disable write protect

15d: enable permanent write protect; if this command is issued, the card/drive will be in a permanent write protected state which cannot be disabled by issuing command 13.

All other command codes are reserved for future use.

07 CIS Specification

This section describes the Card Information Structure (CIS) for the Cactus Technologies PC Cards.

Table 7-26. Card Information Structure

Attribute Offset	Data	1	2	3	4	5	6	7		Description of Contents	CIS Function
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	03h									Link is 3 bytes	Link to next Tuple
004h	D9h	Dev ID Type Dh = I/O				W 1	Speed 1h = 250ns			I/O Device, No WPS, 250ns	Device ID, WPS, Speed
006h	01h	1x					2K units			2 Kilobytes of Address Space	Device Size
008h	FFh	List End Marker								End of Devices	End Marker
00Ah	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Ch	04h									Link is 4 bytes	Link to next tuple
00Eh	02h	Reserved 0						3 1	M 0	Conditions: Dual voltage card, 3V operation is allowed, and WAIT is not used	3 Volts Operation, Wait Function
010h	D9h	Dev ID Type Dh = I/O				W 1	Speed 01h=250nsec			I/O Device, No WPS, Speed is 250 nsec with Wait	Device ID, WPS, Speed
012h	01h	1x					2K units			2Kilobytes of Address Space	Device Size
014h	FFh	List End Marker								End of Devices	End Marker
016h	18h	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
018h	02h									Link is 2 bytes	Link Length
01Ah	DFh	PCMCIA JEDEC Manufacturer's ID								First Byte of JEDEC ID for Cactus PC Card-ATA 12V	Byte 1, JEDEC ID of Device 1 (0-2K)
01Ch	01h	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2, JEDEC ID
01Eh	20h	CISTPL_MANFID								Manufacturer's ID Tuple	Tuple Code

020h	04h								Link is 4 bytes	Link Length
022h	00h	Low Byte of PCMCIA Manufacturer's Code							JEDEC Manufacturer's ID	Low Byte of PCMCIA Mfg ID
024h	00h	High Byte of PCMCIA Manufacturer's Code							Code of 0 because other byte is JEDEC 1 byte Manufacturer's ID	High Byte of PCMCIA Mfg ID
026h	00h	Low Byte of Product Code							Manufacturer specific info	Low Byte Product Code
028h	00h	High Byte of Product Code							Manufacturer specific info	High Byte Product Code
02Ah	21h	CISTPL_FUNCID							Function ID Tuple	Tuple Code
02Ch	02h								Link length is 2 bytes	Link to next tuple
02Eh	04h	Function Type Code							Disk Function	Function Code
030h	01h	R 0	R 0	R 0	R 0	R 0	R 0	R 0	P 1	Attempt installation at Post P: Install at POST R: Reserved (0)	
032h	22h	CISTPL_FUNCE							Function Extension Tuple	Tuple Code
034h	02h								Link length is 2 bytes	Link to next tuple
036h	01h	Disk Function Extension Tuple Type							Extension tuple describes the Interface Protocol	Extension Tuple Type for Disk
038h	01h	Interface Type Code							PC Card-ATA Interface	Extension Info
03Ah	22h	CISTPL_FUNCE							Function Extension tuple	Tuple Code
03Ch	03h								This tuple has 3 info bytes	Link Length
03Eh	02h	Disk Function Extension Tuple Type							Basic PCMCIA-ATA Extension tuple	Extension Tuple Type for Disk
040h	04h	R 0	R 0	R 0	R 0	U 0	S 1	V 0		No Vpp, Silicon Drive with no Unique Manufacturer/Serial Number combined string V=0:No Vpp Required S:Silicon, else Rotating U:ID Drive Mfg/SN not Unique	Basic ATA Option Parameters
042h	07h	R 0	I 0	E 0	N 0	P3 0	P2 1	P1 1	P0 1	All power down modes and power commands are not needed to minimize power. P0:Sleep Mode Supported P1:Standby Mode Supported P2:Idle Mode Supported P3:No Drive Auto Power Control N:Some Config includes 3X7 E:Index Bit not Emulated I:Twin -IOis16 unspecified	Extended ATA Option Parameters
044h	1Ah	CISTPL_CONF							Configuration Tuple	Tuple Code

046h	05h									Link Length is 5 bytes	Link to next tuple
048h	01h	RFS 00			RMS 00			RAS 01		Size of Reserved Field is 0 bytes, Size of Register Mask is 1 Byte, Size of Config Base Address is 2 bytes RFS:Bytes in Reserved Field RMS:Bytes in Reg Mask-1 RAS:Bytes in Base Addr-1	Size of fields byte (TPCC_SZ)
04Ah	07h	TPCC_LAST								Entry with Config Index of 07h is final entry in table	Last entry of configuration table
04Ch	00h	TPCC_RADR (lsb)								Configuration Registers are	Location of
04Eh	02h	TPCC_RADR (msb)								located at 200h in Reg Space.	Config Registers
050h	0Fh	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	First 4 Configuration Registers are present I:Configuration Index C:Configuration and Status P:Pin Replacement S:Socket and Copy R:Reserved for future use	TPCC_RMSK
052h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
054h	0Bh									Link to next tuple is 11 bytes. Also limits size of this tuple to 13 bytes.	Link to next tuple
056h	C0h	I 1	D 1	Configuration Index 0						**Memory Mapped I/O Configuration** Configuration Index for this entry is 0. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
058h	C0h	W 1	R 1	P 0	B 0	Interface Type 0				Memory Only Interface(0), Bvd's and wProt not used, Ready/-Busy and Wait for memory cycles active. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF

05Ah	A1h	M 1	MS 1		IR 0	IO 0	T 0	P 1			Vcc only Power; No Timing, I/O, or IRQ; 2 Byte Mem Space Length; Misc Entry Present P:Power info type T:Timing info not present IO:I/O space not used IR:Interrupt not used MS:Mem space info type M:Misc info byte(s) present	TPCE_FS
05Ch	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1		Nominal Voltage Follows NV:Nominal Voltage info present LV:Mimimum Voltage info present HB:Maximum Voltage info present SI:No Static Current info AI:No Average Current info PI:Peak Current info present DI:No Power Down Current info	Power Parameters for Vcc
05Eh	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V				Vcc Nominal is 5 Volts	Vcc Nominal Value
060h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V				Vcc Minimum is 4.5 Volts	Vcc Minimum Value
062h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V				Vcc Maximum is 5.5 Volts	Vcc Maximum Value
064h	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10				Peak Current is 80 mA	Peak Current
066h	08h	Length in 256 bytes pages (lsb)									Length of Mem Space is 2 KB	TPCE_MS Length LSB
068h	00h	Length in 256 bytes pages (msb)									Start at 0 on card	TPCE_MS Length MSB
06Ah	21h	X 0	R 0	P 1	RO 0	A 0	T 1				Power Down, and Twun Card. T: Twin Cards Allowed is 1 A: Audio Not Supported RO: Read/Write Mode P: Power Down Supported R: Reserved X: No more Misc Fields Bytes	TPCE_MI
06Ch	1Bh	CISTPL_CE									Configuration Entry tuple	Tuple code
06Eh	06h	CISTPL_LINK									Link to next tuple is 6 bytes	link to next tuple
070h	00h	ID Configuration Index									Memory mapped configuration, index=0	TCPCE_INDX
072h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1			P:Power info type No Vpp	TPCE_FS
074h	21h	R 0	DI 0	PI 1	AI 0	SI 0	H 0	LV 0	NV 1		PI:Peak Current Info NV:Nominal Operation Supply Voltage Info	TPCE_PD

076h	B5h	X 1	Mantissa 6h = 3.0		Exponent 5h = 1		Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
078h	1Eh	X 0	1Eh				+.30	Nominal Operation Supply Voltage Extension Byte
07Ah	4Dh	X 0	Mantissa 9h = 4.5		Exponent 5h = 10		Max Average Current over 10 msec is 45mA	Max Average Current
07Ch	1Bh	CISTPL_CE					Configuration Entry Tuple	Tuple Code
07Eh	0Dh						Link to next tuple is 13 bytes. Also limits size of this tuple to 15 bytes.	Link to next tuple
080h	C1h	I 1	D 1	Configuration Index 1			**I/O Mapped Contiguous 16 registers configuration** Configuration Index for this entry is 1. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDX
082h	41h	W 0	R 1	P 0	B 0	Interface Type 1	I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
084h	99h	M 1	MS 0	IR 1	IO 1	T 0	M: misc info present MS: no memory space info IR: Interrupt used IO: I/O space used T: No Timing info	Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present

086h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage info LV:Mimimum Voltage info HB:Maximum Voltage info SI:No Static Current info AI:No Average Current info PI:Peak Current info DI:No Power Down Current info	Power Parameters for Vcc
088h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
08Ah	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Minimum is 4.5 Volts	Vcc Minimum Value
08Ch	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Maximum is 5.5Volts	Vcc Maximum Value
08Eh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
090h	64h	R 0	S 1	E 1	IO AddeLines 4					Supports both 8 and 16 bit I/O hosts. 4 Address lines and no range so 16 registers and host must do all selection decoding. IOAddrLines:4 addresses decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
092h	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present V:No Vendor Unique IRQ B:No Bus Error IRQ I:No IO Check IRQ N:No Non-Maskable IRQ	TPCE_IR
09Ah	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
09Ch	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
09Eh	01h	I 0	D 0	Configuration Index 1						I/O mapped contiguous 16 3.3V configuration	TPCE_INDX
0A0h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type No Vpp	TPCE_FS

0A2h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current Info NV:Nominal Operation Supply Voltage Info	Power Parameters for Vcc
0A4h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
0A6h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0A8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45 mA	Max Average Current
0AAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0ACh	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple
0AEh	C2h	I 1	D 1	Configuration Index 2						**AT Fixed Disk Primary I/O Address Configuration** Configuration Index for this entry is 2. Interface Byte follows this byte. Default Configuration	TPCE_INDX
0B0h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Not Used for Memory Cycles	TPCE_IF
0B2h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Description; No Timing; I/O and IRQ present; No Mem Space; Misc Entry present P:Power info type T:No Timing info present IO:I/O port info present IR:Interrupt info present MS:No Mem space info M:Misc info byte(s) present	TPCE_FS
0B4h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage LV:Mimimum Voltage HB:Maximum Voltage SI:No Static Current info AI:No Average Current info PI:Peak Current DI:No Power Down Current info	Power Parameters for Vcc
0B6h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value

0B8h	4Dh	X 0	Mantissa 9h = 4.5			Exponent 5h = 1V	Vcc Minimal is 4.5Volts	Vcc Minimum Value
0BAh	5Dh	X 0	Mantissa Bh = 5.5			Exponent 5h = 1V	Vcc Maximum is 5.5Volts	Vcc Maximum Value
0BCh	75h	X 0	Mantissa Eh = 8.0			Exponent 5h = 10	Max Average Current over 10 msec is 80 mA	
0BEh	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10		Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (1F0-1F7, 3F6-3F7) on A9 through A0 for I/O cycles. IO AddrLines10 lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0C0h	61h	LS 1		AS 2	N Ranges - 1 1		Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
0C2h	F0h	1st I/O Base Address (lsb)					First I/O Range base is	
0C4h	01h	1st I/O Base Address (msb)					1F0h	
0C6h	07h	1st I/O Range Length - 1					8 bytes total ==>1F0-1F7h	I/O Length - 1
0C8h	F6h	2nd I/O Base Address (lsb)					2nd I/O Range base is	
0CAh	03h	2nd I/O Base Address (msb)					3F6h	
0CCh	01h	2nd I/O Range Length - 1					2 bytes total ==>3F6-3F7h	I/O Length - 1
0CEh	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14	IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Not Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR

0D0h	21h	X 0	R 0	P 1	RO 0	A 0	T 1	Power-Down, and Twin Card. T:Twin Cards Allowed is 1 A:Audio Not Supported RO:Read/Write Mode P:Power Down Supported R:Reserved X:No More Misc Fields Bytes	TPCE_MI
0D2h	1Bh	CISTPL_CE						Configuration Entry Tuple	Tuple Code
0D4h	06h							Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
0D6h	02h	I 0	D 0	Configuration Index 3				AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
0D8h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1	P:Power info type	TPCE_FS
0DAh	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
0DCh	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
0DEh	1Eh	X 0	1Eh				+.30			Nominal Operation Supply Voltage Extension Byte	
0E0h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
0E2h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0E4h	12h									Link to next tuple is 4 bytes.	Link to next tuple
0E6h	C3h	I 0	D 0	Configuration Index 3						**AT Fixed Disk Secondary I/O Address Configuration** Configuration Index for this entry is 3. Interface Byte follows this byte. Default Configuration	TPCE_INDX
0E8h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Not Used for Memory Cycles	TPCE_IF

0EAh	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present. P:Power info type T:No Timing info present IO:I/O port info present IR:Interrupt info present MS:No Mem space info type M:Misc info byte(s) present	TPCE_FS
0ECh	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage info LV:Mimimum Voltage info HV:Maximum Voltage info SI:No Static Current info AI:No Average Current info PI:Peak Current DI:No Power Down Current info	Power Parameters for Vcc
0EEh	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			Vcc Nominal is 5Volts	Vcc Nominal Value
0F0h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			Vcc Minimum is 4.5Volts	Vcc Minimum Value
0F2h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			Vcc Maximum is 5.5Volts	Vcc Maximum Value
0F4h	75h	X 0	Mantissa Eh = 1.0				Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current
0F6h	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (170-177, 376-377) on A9 through A0 for I/O cycles. IO AddrLines10 lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0F8h	61h	LS 1	AS 2	N Ranges–1 1						Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
0FAh	70h	1st I/O Base Address (lsb)								First I/O Range base is	
0FCh	01h	1st I/O Base Address (msb)								170h	
0FEh	07h	1st I/O Range Length - 1								8 bytes total ==>170-177h	I/O Length - 1
100h	76h	2nd I/O Base Address (lsb)								2nd I/O Range base is	
102h	03h	2nd I/O Base Address (msb)								376h	

104h	01h	2nd I/O Range Length - 1								2 bytes total ==>376-377h	I/O Length - 1
106h	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Not Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
108h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T:Twin Cards Allowed is 1 A:Audio Not Supported RO:Read/Write Mode P:Power Down Supported R:Reserved X:No More Misc Fields Bytes	TPCE_MI
10Ah	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
10Ch	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple
10Eh	03h	I 0	D 0	Configuration Index 3						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
110h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P:Power info type	TPCE_FS
112h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc
114h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
116h	1Eh	X 0	1Eh				+.30			Nominal Operation Supply Voltage Extension Byte	
118h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max Average Current over 10 msec is 45mA	Max Average Current
11Ah	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
11Ch	04h									Link to next tuple is 4 bytes.	Link to next tuple
11Eh	07h	I 0	D 0	Configuration Index 7						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
120h	00h	M 0	MS 0		IR 0	IO 0	T 0	P 0		P:Power info type	TPCE_FS

122h	028h		Cactus Specific Code	Reserved
124h	0D3h		Cactus Specific Code	Reserved
126h	014h	CISTPL_NO_LINK	Prevent Scan of Common Memory	Tuple Code
128h	000h	CISTPL_LINK	Link Length is 0 Bytes	Link to next tuple
12Ah	015h	CISTPL_VERS_1	Level 1 version/product info	Tuple Code
12Ch	022h	CISTPL_LINK	Link Length is 24h bytes	Link to next tuple
12Eh	004h	TPPLV1_MAJOR	PCMCIA 2.0/JEIDA 4.1	Major Version
130h	001h	TPPLV1_MINOR	PCMCIA 2.0/JEIDA 4.1	Minor Version
132h	030h		0	Info String 1
134h	030h		0	
136h	030h		0	
138h	030h		0	
13Ah	030h		0	
13Ch	030h		0	
13Eh	030h		0	
140h	030h		0	
142h	030h		0	
144h	000h		Null Terminator	
146h	043h		C	Info String 2
148h	061h		a	
14Ah	063h		c	
14Ch	074h		t	
14Eh	075h		u	
150h	073h		s	
152h	020h		‘space’	
154h	04Bh		K	
156h	043h		C	
158h	033h		3	
15Ah	030h		0	
15Ch	033h		3	
15Eh	020h		‘space’	
160h	056h		V	
162h	065h		e	
164h	072h		r	
166h	031h		1	
168h	02Eh		.	
16Ah	030h		0	
16Ch	030h		0	
16Eh	000h		Null Terminator	
170h	0FFh	CISTPL_END	End of CISTPL_VER_1	End Marker
172h	0FFh	CISTPL_END	End of CIS	Tuple Code

Model KPXYZT-303P1

Where X is card capacities:

128M	128MB
256M	256MB
512M	512MB
1G	1GB
2G	2GB
4G	4GB
8G	8GB
16G	16GB
32G	32GB

Where Y is card configuration

R	Removable card
F	Fixed card

Where T is NAND type

Blank	Samsung (for all capacities other than 32GB)
T	Toshiba (only for 32GB)

If your systems cannot accept bootable removed PC card (R), then please order Fixed PC Card (F).

Where Z is temperature

Blank	Standard temperature (0° C to +70° C)
I	Extended temperature (-45° C to +90° C)

Where P1 is firmware option

Blank	Standard firmware
P1	Pro Series firmware

Example:

1. 512MB PC Card Removable KP512MR-303
2. 1GB PC Card Removable Extended Temp KP1GRI-303
3. 2GB PC Card Fixed, Pro option KP2GF-303P1
4. 128MB PC Card Fixed Extended Temp KP128MFI-303

Cactus Technologies® Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong

Tel: +852-27972261
Fax: +852-27973777
Email: tech@cactus-tech.com

Cactus Technologies® Limited
Santa Clara, CA 95054
Email: tech@cactus-tech.com

Appendix C

Cactus Technologies® Worldwide Sales Offices

Cactus Technologies® Limited

Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong

Tel: +852-27972277
Fax: +852-27973777
Email: sales@cactus-tech.com

Cactus® USA

3112 Windsor Road
Suite A-356
Austin, Texas

Tel: +512-775-0746
Email: americas@cactus-tech.com

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies®' responsibilities regarding the Cactus Technologies® Industrial Grade PC Card. In satisfaction of its obligations hereunder, Cactus Technologies®, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

Cactus Technologies®' products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing or replacing the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty

shall be tested to the product s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

Cactus Technologies® reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

Cactus Technologies® may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, Cactus Technologies® also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product s specifications.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

Cactus Technologies® Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong